CLAIMS

1. A data communications interface for a node of a data processing network, the interface comprising:

a transmission channel for communicating data from the node to the network;

a transmission processor connected to the transmission channel for controlling flow of data through the transmission channel;

a reception channel for communicating data from the network to the node;

a reception processor connected to the reception channel for controlling flow of data through the reception channel;

a shared memory; and,

a local bus providing access to the shared memory by the transmission and reception processors.

2. An interface as claimed in claim 1 wherein the shared memory comprises a store for control information to be used by the transmission and reception processors in controlling said flows of data.

3. An interface as claimed in claim 1 ~~or claim 2,~~ comprising a communication path for communicating information between the transmission and reception processors via the shared memory.

4. An interface as claimed in ~~any preceding claim~~ claim 1 comprising bus interface logic for connecting the local bus, the transmission data channel, and the reception data channel to a bus architecture of the node.

5. An interface as claimed in ~~any preceding claim~~ claim 1, comprising:

a transmission control path;

transmission segmentation logic for receiving a data frame, comprising a transmission header and a transmission payload, from the node and supplying the transmission payload to the transmission channel and the transmission header to the transmission control path;

the transmission processor being located in the transmission control path for controlling communication of data from the transmission payload to the network via the transmission channel in dependence on the transmission header;

a reception control path;

reception segmentation logic for receiving a data packet, comprising a reception header and a reception payload, from the network and supplying the reception payload to the reception channel and the reception header to the reception control path; and,

the reception processor being located in the reception control path for controlling communication of data from the reception payload to the node via the reception channel in dependence on the reception header.

6. A network interface card for insertion into a computer system, the network interface card comprising a printed circuit board and a data communications interface as claimed in ~~any preceding claim~~ claim 1 mounted on the printed circuit board.

7. An application specific integrated circuit comprising an interface as claimed in ~~any of claims 1 to 5.~~ claim 1

8. A computer system comprising: a cental processing unit; a memory; a data communications interface as claimed in ~~any of claims 1 to 5~~ claim 1; and, a bus architecture interconnecting the central processing unit, the memory, and the data communications interface.

9. A data processing network comprising a plurality of computer systems as claimed in claim 8 and a network architecture interconnected the computer systems.

Rule 1.126

10 M. A method for communicating data to and from a node of a data processing network, the method comprising:

communicating data from the node to the network via a transmission channel;

controlling flow of data through the transmission channel via a transmission processor connected to the transmission channel;

communicating data from the network to the node via a reception channel;

controlling flow of data through the reception channel via a reception processor connected to the reception channel; and,

providing access to a shared memory by the transmission and reception processors via a local bus.

Rule 1.126

11 ~~12~~. A method as claimed in claim ~~11~~ 10, comprising storing, in the shared memory, control information to be used by the transmission and reception processors in controlling said flows of data.

Rule 1.126

A 10 ~~13~~ 12. A method as claimed in ~~claim 10 or~~ claim ~~11~~ 10, comprising communicating, via the shared memory, information between the transmission and reception processors.